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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,850	08/21/2003	Mahito Shinohara	03500.017485	6157

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EXAMINER	
PRABHAKHER, PRITHAM DAVID	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,850	SHINOHARA, MAHITO	
	Examiner	Art Unit	
	Pritham Prabhakher	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8,11 and 14* is/are rejected.

7)☒ Claim(s) *4-7,9,10,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/24/2004 and 12/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because

The numbers to the devices are misnumbered.

Correction is required. See MPEP § 608.01(b).

Claim Objections

Claim1 is objected to because of the following informalities:

In Line 11, the word "a" should precede the word first. In Line 13, the word "an" should precede the word electrode. In Line 16, the word "a" should precede the word second. In Line 18, the word "the" should precede the word same, and the word "a" should precede the word semiconductor. Also, the word "a" should be deleted before the words "junction-type" in Lines 21 and 26.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,8,11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US Patent No.: 6163023) and further in view of Orava et al. (US Pub No.: 2001/0001562A1).

*In regard to **Claim 1**, Watanabe teaches of an image pickup device including an array of a plurality of pixels including photoelectric conversion portions for accumulating signal charges generated by photoelectric conversion and an amplifying transistor for amplifying the signal charges generated by said photoelectric conversion portion to output the amplified signal charges **(Column 1, Lines 9-20)**, said device comprising:*

*a junction-type field effect transistor, including a main electrode made of first semiconductor region of a first conduction type connected to control electrode region of said amplifying transistor (Looking at Figure 1A, the transistor 4 has an end (semiconductor region of first conduction type) connected to the gate 1G of the amplifying transistor 1, **Column 7, Line 15)** included in two pixels adjacent to each other **(Figure 10** shows two pixels, 100, that are adjacent to each other**)** and a control electrode region made of second semiconductor region of a second conduction type opposite to the first conductive type (The region between 1G and 10P is the control electrode region. It is made of a second semiconductor region (the gate 1G has a different semiconductor region) that is opposite to the switch end of the region of transistor 4 (first conductive type)) having same electric potential as that of semiconductor region of the second conduction type included in a semiconductor region forming said photoelectric conversion portions (The semiconductor region of a second conduction type 1G has the same electric potential as the semiconductor region of the*

photoelectric conversion portion (anode of diode 10P), because the gate 1G is linked to it, Figure 1A), said a junction-type field effect transistor connecting said first semiconductor region in series (Figure 1A shows that the connection is a series connection); and

an electric potential supplying circuit for supplying predetermined electric potential to the main electrode region of said a junction-type field effect transistor (Looking at Figure 1A and Figure 10, Wiring Tx(i) and Tx(i + 1) (electric potential supplying circuit) is capable of supplying a predetermined electric potential to the transistors).

Although Watanabe teaches of MOSFET's, the reference does not teach that the Field Effect Transistors are Junction Type Field Effect Transistors (JFET's). Orava et al. teach that Field Effect Transistors can be implemented with either JFET of MOSFET, ***Paragraph 0143 of Orava et al****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate into the teachings of Watanabe, a JFET instead of a MOSFET because depending on the charge storage time and radiation hardness requirements, appropriate technologies such as JFET or MOSFET can be used,* ***Paragraph 0143 of Orava et al.***

Regarding ***Claim 2****, Watanabe and Orava et al. disclose an image pickup device according to claim 1, further comprising a transferring transistor for transferring the signal charges accumulated in said photoelectric conversion portion included in said pixel (The transistor 3 is used to transfer the signal charges that were accumulated in the p-n junction photodiode 10 (photoelectric conversion portion). It is only when the*

third transistor 3 is turned on that the amplifier (transistor 4) amplifies the signal charge stored in the photodiode 10 and the amplified signal is read out (transferred) through the transistor 3 to the signal line 13, ***Column 7, Lines 46-64 of Watanabe)****.*

With regard to ***Claim 3****, Watanabe and Orava et al. disclose an image pickup device according to claim 1, wherein said first semiconductor region constitutes a part of said photoelectric conversion portion (The first semiconductor region (the switch end of the fourth transistor) is also connected to the P-type electrode 10p of the photodiode 10 (photoelectric conversion portion),* ***Figure 1A of Watanabe)****.*

Regarding ***Claim 8****, Watanabe and Orava et al. disclose an image pickup device according to claim 1, wherein said potential supplying circuit (Tx(i) and Tx(I+1)) can selectively supply first electric potential (Logic High) and second electric potential (Logic Low) different from the first electric potential (See Tx(i) and Tx(I+1) in* ***Figure 11 of Watanabe)****, said image pickup device further comprising a first driving circuit (Vertical Scan circuit 102) for controlling said potential supplying circuit (Figure 10 of Watanabe shows that the VSC 102 controls Tx(i) and Tx (i+1)) so as to supply the first electric potential to a plurality of the pixels from which signals are read (Figures 10 and 11 of Watanabe show that the first electric potential (Logic High) can be supplied to a plurality of pixels 100), and to supply the second electric potential to a plurality of the pixels from which no signals are read (The second electric potential (Logic Low) can be supplied to a plurality of pixels 100 as well,* ***Figure 2 of Watanabe****. Also, Figure 11 shows that*

when Tx goes low (second electric potential), no charge is read out, ***Column 7, Lines 45-55 of Watanabe)****.*

In regard to ***Claim 11,*** *Watanabe teaches of an image pickup device including an array of a plurality of pixels including photoelectric conversion portions for accumulating signal charges generated by photoelectric conversion, an amplifying transistor for amplifying the signal charges generated by said photoelectric conversion portion to output the amplified signal charges* ***(Column 1, Lines 9-20)****, and a junction-type field effect transistor comprising:*

a first main electrode made of first semiconductor region of a first conduction type connected to control electrode region of said amplifying transistor (Looking at Figure 1A, the transistor 4 has an end (semiconductor region of first conduction type) connected to the gate 1G of the amplifying transistor 1, ***Column 7, Line 15)****, a control electrode region made of second semiconductor region of a second conduction type opposite to the first conductive type (The region between 1G and 10P is the control electrode region. It is made of a second semiconductor region (the gate 1G has a different semiconductor region) that is opposite to the switch end of the region of transistor 4 (first conductive type))) having same electric potential as that of semiconductor region of the second conduction type included in a semiconductor region forming said photoelectric conversion portions (The semiconductor region of a second conduction type 1G has the same electric potential as the semiconductor region of the photoelectric conversion portion (anode of diode 10P), because the gate 1G is linked to*

it, Figure 1A), and a second main electrode made of third semiconductor region of a first conduction type (The switch portion of transistor 1 has a first conduction type) connected to a potential supply portion (it is connected through transistor 3 to the supply potential wiring Tx) for supplying a predetermined electric potential (Looking at Figure 1A and Figure 10, Wiring Tx(i) and Tx(i + 1) (electric potential supplying circuit) is capable of supplying a predetermined electric potential to the transistors).

Although Watanabe teaches of MOSFET's, the reference does not teach that the Field Effect Transistors are Junction Type Field Effect Transistors (JFET's). Orava et al. teach that Field Effect Transistors can be implemented with either JFET of MOSFET, ***Paragraph 0143 of Orava et al****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate into the teachings of Watanabe, a JFET instead of a MOSFET because it requires less space and can be easily programmed.*

Regarding ***Claim 14****, Watanabe and Orava et al. disclose an image pickup system comprising:*

an image pickup device defined in claim1;

a lens for focusing light onto said plurality of pixels (It is inherent that a lens is present for focusing light onto the pixels because a lens is needed to help capture and store an image in conjunction with the main body of the camera)

an analog-to-digital conversion circuit for converting signals from said plurality of pixels to digital signals (an (ADC) for converting charge read from a pixel circuit into a digital charge value, ***Paragraph 0041 of Orava et al.);*** *and*

a signal processing circuit for processing signals from said analog-to-digital conversion circuit ***(Figure 3 of Orava et al.*** *shows a signal processing circuit 58 for processing signals from the A/D converter)*.

Allowable Subject Matter

Claims 4-7,9-10, 12,13 are objected to as being dependent upon a rejected base claims 1 and 11, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pritham Prabhakher whose telephone number is 571-270-1128. The examiner can normally be reached on M-F (7:30-5:00) Alt Friday's Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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